

REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated June 20, 2005 has been received and its contents carefully reviewed. Applicant appreciates the Examiner's indication of allowability of claim 26.

Claims 1, 4, 7, 8, 11, 14, 15, 22 and 23 are hereby amended. Claims 15 and 22 are herein amended to correct discrepancies in previously presented amendments. Claims 1 and 11 are herein amended to include the limitations of claims 2 and 12, respectively. Claims 2, 10, 12 and 25 are hereby cancelled. Accordingly, claims 1, 3-9, 11, 13-24 and 26 are pending. Reexamination and reconsideration of the pending claims are respectfully requested.

In the Office Action, claims 8 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 8 and 23 are herein amended to include the limitations of the base claim. Accordingly, Applicant respectfully requests the withdrawal of this objection.

Additionally, in the Office Action, claims 1-7, 9-18, 20-22, 24 and 25 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,817,549 to Yamazaki et al. (hereinafter "Yamazaki"). Claim 19 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Stanley Wolf, Silicon Processing for The VLSI Era, Vol. II, 1986, p.436. (hereinafter "the Wolf document").

The rejection of claims 1-7, 9-18, 20-22, 24 and 25 as being anticipated by Yamazaki is respectfully traversed and reconsideration is requested.

Claim 1 is allowable over Yamazaki in that claim 1 recites a combination of elements including, for example, "depositing silicon oxide over the polysilicon active layer to form a gate insulation layer under a vacuum condition; applying heat to anneal the gate insulation layer under the vacuum condition, wherein there is no vacuum break between depositing silicon oxide to form the gate insulation layer and applying heat to anneal the gate insulation layer."

Yamazaki does not teach at least these features of the claimed invention. Specifically, the method of claim 1 of the present application is different from the method of Yamazaki in that the “gate insulation layer” is formed “under a vacuum condition” and “there is no vacuum break between depositing silicon oxide to form the gate insulation layer and applying heat to anneal the gate insulation layer.” In contrast, Yamazaki teaches that after the gate insulating film had been formed, it was subjected to an annealing treatment by first locating the substrate in the thermal annealing apparatus as shown in Figure 1. See column 12, lines 56-63. Because the substrate is located in a thermal annealing apparatus after the gate insulating layer is formed, the vacuum condition present when the silicon oxide layer was deposited is broken. Furthermore, Yamazaki teaches that the pressure in the reaction chambers is set to 1 atmosphere. See column 13, lines 6-9. This also indicates that the vacuum condition is broken in Yamazaki. Accordingly, because Yamazaki fails to teach these features of claim 1, Applicant respectfully submits that claim 1 and claims 3-7 and 9, which depend therefrom, are allowable over Yamazaki. Also, claims 2 and 10 are cancelled, therefore, the rejection of claims 2 and 10 is moot.

Similarly, claim 11 is allowable over Yamazaki in that claim 11 recites a combination of elements including, for example, “depositing silicon oxide over the polysilicon active layer to form a gate insulation layer under a vacuum condition; applying heat to anneal the gate insulation layer under the vacuum condition, wherein there is no vacuum break between depositing silicon oxide to form the gate insulation layer and applying heat to anneal the gate insulation layer.” Yamazaki does not teach at least these features of the claimed invention. Specifically, the method of claim 11 of the present application is different from the method of Yamazaki in that the “gate insulation layer” is formed “under a vacuum condition” and “there is no vacuum break between depositing silicon oxide to form the gate insulation layer and applying heat to anneal the gate insulation layer.” In contrast, Yamazaki teaches that after the gate insulating film had been formed, it was subjected to an annealing treatment by first locating the substrate in the thermal annealing apparatus as shown in Figure 1. See column 12, lines 56-63. Because the substrate is located in a thermal annealing apparatus after the gate insulating layer is formed, the vacuum condition present when the silicon oxide layer was deposited is broken. Furthermore, Yamazaki teaches that the pressure in the reaction chambers is set to 1 atmosphere. See column 13, lines 6-9. This also indicates that the vacuum condition is broken in Yamazaki.

Accordingly, because Yamazaki fails to teach these features of claim 11, Applicant respectfully submits that claim 11 and claims 13-18, 20-22, and 24, which depend therefrom, are allowable over Yamazaki. Also, claims 12 and 25 are cancelled, therefore, the rejection of claims 12 and 25 is moot.

The rejection of claim 19 as being unpatentable over Yamazaki in view of the Wolf document is respectfully traversed and reconsideration is requested.

Applicant respectfully submits that the Wolf document fails to cure the aforementioned defects associated with the teachings of Yamazaki. None of the cited references, singly or in combination, teaches or suggests "depositing silicon oxide over the polysilicon active layer to form a gate insulation layer under a vacuum condition; applying heat to anneal the gate insulation layer under the vacuum condition, wherein there is no vacuum break between depositing silicon oxide to form the gate insulation layer and applying heat to anneal the gate insulation layer," as recited in independent claim 11. In addition, Applicant respectfully submits that there is no motivation for one of ordinary skill in the art to combine the cited references and arrive at the claimed invention with any reasonable expectation of success. Applicant further respectfully submits that the motivation to combine the references comes from the present invention and not from the cited references, which is impermissible. For at least this reason, claim 19, which depends from claim 11, is allowable over the cited references.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the

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filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

The undersigned hereby signs this filing under the authority provided by 37 C.F.R. §1.34 pending the filing of a Power of Attorney and Statement under 3.73(b) executed by Assignee.

Dated: September 16, 2005

Respectfully submitted,

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